Performance Improvement in FPGA-based Data Acquisition Systems using PCI-Express

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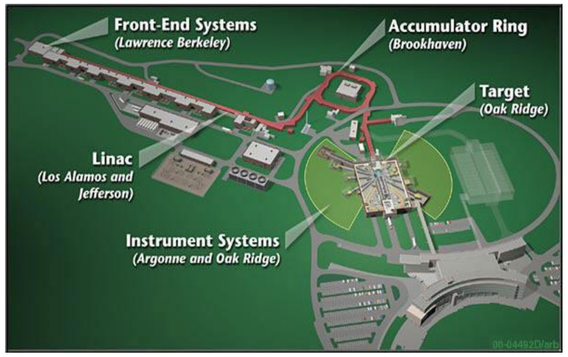
Introduction

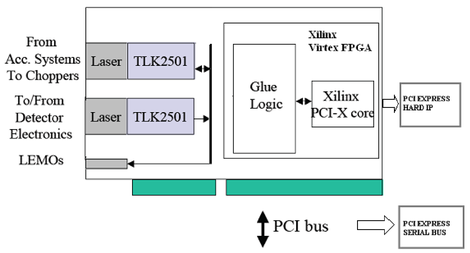
High-speed data acquisition systems stand to benefit from the high-bandwidth serial I/O connectivity provided by PCI-Express. PCI-Express is scalable and supports bi-directional rate of 500 Mbps, to a combined total of up to 16Gbps. In this poster we present a case study of a Timing Module/Optical Communications card redesign at Oak Ridge National Laboratory's Spallation Neutron Source (SNS).



SNS Instrument Systems at ORNL

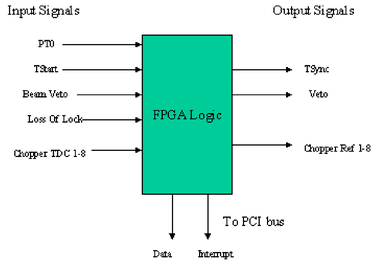
SNS Timing Module

The existing PCI-X based timing module is a data acquisition system used by the instrument systems at the SNS neutron scattering facility.



SNS Timing Module Block Diagram

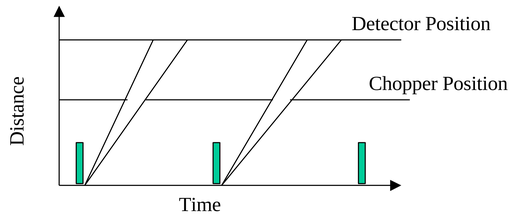
The figure above shows the blocks within the timing module, which consists of two optical transceivers, an Xilinx Virtex-II FPGA that handles glue logic and the PCI interface implemented via Xilinx PCI-X LogiCore.



Signals To/From Glue Logic

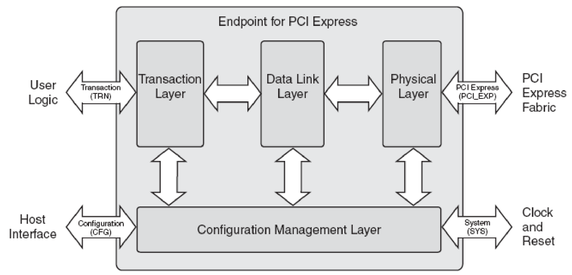
The timing module provides timing signals used by the detector electronics of the instrument systems in addition to other information that can be used to process data. The timing module also provides the master timing pulse to the chopper control system for phasing the chopper disk with the proton-on-target event.

All of the SNS instruments use time-of-flight (TOF) measurements to determine the energies of the neutrons. The TOF is determined by summing the time stamp made at the detector electronics and a constant offset that is determined by the timing module.



Showing operation in a single frame

The figure above shows a representation of a short instrument operating in the first frame. The green pulses on the time axis represent the proton-on-target time. For "no loss of data", neutrons must be detected before the next neutron pulse is generated.



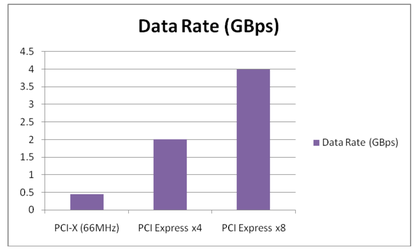
Endpoint Internal Blocks

Using the current timing module, the data acquisition system could only be scaled to higher rates by adding complete PC systems with additional interface cards. In the redesign, we consider the Xilinx Virtex 5 which offers an embedded PCI-Express Hard IP core for high-density, low power communication, and provides many more logic resources for additional expandability and scalability.

Data acquisition systems for instruments in Spallation Neutron Source (SNS) require more than 1 GBps sustained data rate to avoid loss of data. The PCI-Express x4 configuration provides a suitable sustained bidirectional data rate of 2 GBps. If additional bandwidth is required, designs can be scaled to x8 lane width configuration in the same server systems by reconfiguring the FPGA.

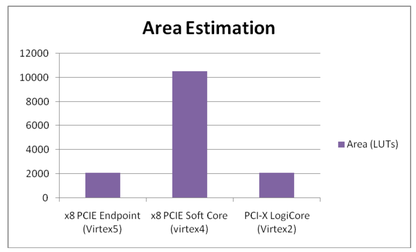
Addressing Current Design Limitations

The 66 MHz PCI-X bus interface does not provide adequate bandwidth for neutron data collection and as a result, timing data is sometimes lost. In our new design, approximately 55 posted writes are transmitted at 512 bytes (Maximum Payload Size) each on x8 link. So the total number of bytes transferred will be 28160 bytes. The transfer time for 512 byte, 32-bit addressable memory write is 13,392 ns. So the total bandwidth achieved in our design with PCI-Express x8 will be 2.1 GBps.



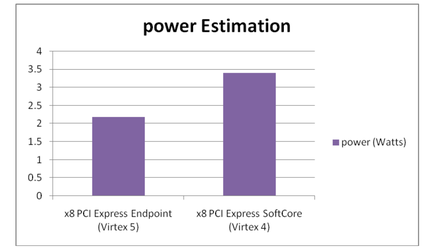
Performance Comparison

Due to the logic area constraints in the Virtex-II FPGA, it is not possible to add more functionality and registers to the current timing board design. However, the logic density and availability of an embedded PCI-Express core in the Virtex 5 allows ample design flexibility and room for expansion. The embedded PCI-Express hardcore in the Virtex 5 requires less area for implementation than a Virtex 4 PCI-Express softcore, or about the same as the PCI-X softcore used in the previous design.



Area Comparison

The figure below shows the power consumption for the PCI-Express implementation in Virtex 5 which is much less than the Virtex 4. The values were taken using Xilinx Power Estimator.



Power Comparison

Approach

Our three stage approach for upgrading the Timing module:

•New Printed Circuit Board Design (includes PCI-Express and Virtex 5 FPGA)

•New FPGA Code Design (using Virtex 5 PCI-Express Endpoint block)

•In-system Debugging and Troubleshooting

Future Work

The future work will include:

•Analysis of performance on the hardware

•Implementation of Bus Master DMA design

•Implement Virtex 5 RocketIO GTP core (to replace TLK transceivers)

Conclusion

There are 24 instrument systems installed in the SNS facility at Oak Ridge National laboratory. In many instrument systems the transfer rate requirement is at least 1GBps to collect all neutron events. Migrating the timing module to Virtex 5 and PCI-Express will not only provide the required throughput but it will also provide enough logic area for future expansion.

References

1.PCI Express Base Specification, v1.1
http://www.pcisig.com/specifications/pciexpress
2.The SNS Facility
http://neutrons.ornl.gov/facilities/facilities_sns.shtml
3.Xilinx Virtex 5 Endpoint Block Plus
http://www.xilinx.com/products/ipcenter/V5_PCI_Express_Block_Plus.htm
4.Understanding Performance of PCI Express System
http://www.xilinx.com/support/documentation/white_papers/wp350.pdf
5.PCI Express Protocol Solutions
http://www.xilinx.com/pcie